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APPLICATION NO.	FILING DATE *	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,845	09/09/2003	Chung-Cheng Chou	252011-1320	5418

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EXAMINER	
LUU, PHO M	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/658,845	CHOU, CHUNG-CHENG	
	Examiner	Art Unit	
	Pho M Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,14-16,24,37-39 and 46-48* is/are rejected.

7)☒ Claim(s) *2-13,17-23,25-36 and 40-45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because the content is written, **"A system for"** and **"Other system are also provided."**. Correction is required. See MPEP § 608.01(b).

Drawings

3. Figure 3 should be designated by a legend such as --**Prior Art**-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction

or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 14-16, 24, 37-39 and 46-48 are rejected under 35 U.S.C. 102(b) as being anticipated by Gonzalez. (US. 5,640,342).

Regarding claim 1, Gonzalez. discloses, in Figure 4 and respective portion of the specification, a four-transistor random access memory cell comprising:

a first transistor (10, Fig. 4) of a first conductivity type (n-type) having a gate (the gate that connects to 16) coupled to a word line (WL) and a source (12) coupled to a bit line;

a second transistor (26, Fig. 4) of the first conductivity type (n-type) having a gate (the gate that connects to node 20) coupled to a drain (connected to 28) of the first transistor (10, Fig. 4) and a source (the source of 26) coupled to receive a first voltage (ground);

a third transistor (22, Fig. 4) of a second conductivity type (p-type) having a gate coupled to a drain (the connection at node 28) of the second transistor (26, Fig. 4), a

source coupled to receive a second voltage (Vcc) and a drain (the connection at node 20) coupled to the drain of the first transistor (10, Fig. 4); and

a fourth transistor (24, Fig. 4) of the second conductivity (p-type) type having a gate (see node 20) coupled to the drain of the first transistor (the drain of transistor 10), a source coupled to receive the second voltage (Vcc) and a drain (the connection at node 28) coupled to the drain of the second transistor (26, Fig. 4).

Regarding to claim 14, Gonzalez. disclosed, in Figure 4 and respective portion of the specification, the four-transistor random access memory cell that wherein the first conductivity type (transistor 22, 24 in Fig. 4 are P-type) and second conductivity type (transistor 10, 26 in Fig. 4 are N-type) are respectively P and N type.

Regarding claim 15, Gonzalez. discloses, in Figure 4 and respective portion of the specification, a random access memory cell comprising:

a first transistor (10, Fig. 4) of a first conductivity type (n-type) having a gate (the gate that connects to 16) coupled to a word line (WL) and a source (12, Fig. 4) coupled to a bit line;

a second transistor (22, Fig. 4) of a second conductivity type (p-type) having a source coupled to receive a second voltage (Vcc) and a drain coupled to the drain (the connection at node 20) of the first transistor (10);

a diode (18, Fig. 4) having an anode coupled to the drain (at node 20) of the first transistor (10, Fig. 4) and a cathode coupled to receive first voltage (Vss or ground); and

an inverter (transistors 24 and 26 formed an inverter) having an input terminal (the connection of gates of transistors 24 and 26) coupled to the drain (at node 20) of the first transistor (10) and an output terminal (node 28, Fig. 4) coupled to a gate of the second transistor (22, Fig. 4).

Regarding to claim 16, Gonzalez. disclosed, in Figure 4 and respective portion of the specification, the random access memory cell, which is the inverter, comprises:

a third transistor (26, Fig. 4) of the first conductivity type (n-type) having a gate coupled to the drain (node 20) of the first transistor (10) and a source coupled to receive the first voltage (Vss or ground); and

a fourth transistor (24, Fig. 4) of the second conductivity type (p-type) having a gate coupled to the drain (at node 20) of the first transistor (10, figure 4), a source coupled to receive the second voltage (Vcc) and a drain (node 28) coupled to the drain the third transistor (26, figure 4).

Regarding claim 24, Gonzalez. discloses, in Figure 4 and respective portion of the specification, a memory device comprising:

a plurality of memory cells (any memory device would includes a plurality of memory cells) wherein data is read from and written (the DRAM of Gonzalez clearly perform the function of reading and writing data) into each of the memory cells through bit lines by control signals on word lines (every memory device must have word lines for selecting an address and bit lines for carrying data), each of the memory cells comprising:

a first transistor (10, Fig. 4) of a first conductivity type (n-type) having a gate coupled to one of the word lines (the connection 16) and a source coupled to one of the bit lines (the connection at 12);

a second transistor (26, Fig. 4) of the first conductivity type (n-type) having a gate coupled to a drain (at node 20) of the first transistor (10) and a source coupled to receive a first voltage (Vss or ground);

a third transistor (22, Fig. 4) of a second conductivity type (p-type) having a gate coupled to a drain (the connection at node 28) of the second transistor (26), a source coupled to receive a second voltage (Vcc) and a drain coupled to the drain of the first transistor (the connection at node 20); and

a fourth transistor (24, Fig.)) of the second conductivity type (P-type) having a gate coupled to the drain (the connection at node 20) of the first transistor (10), a source coupled to receive the second voltage (Vcc) and a drain coupled to the drain (the connection at node 28) of the second transistor (26).

Regarding to claim 37, Gonzalez. disclosed, in Figure 4 and respective portion of the specification, the memory device, which is the first conductivity type (transistor 22, 24 in Fig. 4 are P-type) and second conductivity types (transistor 10, 26 in Fig. 4 are N-type) are P and N type respectively.

Regarding claim 38, Gonzalez. discloses, in Figure 4 and respective portion of the specification, a memory device memory comprising:

a plurality of memory cells (any memory device would includes a plurality of memory cells) wherein data is read from and written (the DRAM of Gonzalez clearly perform the function of reading and writing data) into each of the memory cells through bit lines by control signals on word lines (every memory device must have word lines for selecting an address and bit lines for carrying data), each of the memory cells comprising:

a first transistor (10, Fig. 4) of a first conductivity type (n-type) having a gate coupled to one of the word lines (the connection 16) and a source coupled to a bit lines (the connection at 12);

a second transistor (22, Fig. 4) of a second conductivity type (p-type) having a source coupled to receive a second voltage (Vcc) and a drain coupled to the drain (the connection at node 20) of the first transistor (10);

a diode (18, Fig. 4) having an anode coupled to the drain (at node 20) of the first transistor (10, Fig. 4) and a cathode coupled to receive first voltage (Vss or ground); and

an inverter (transistors 24 and 26 formed an inverter) having an input terminal (the connection of gates of transistors 24 and 26) coupled to the drain (at node 20) of the first transistor (10) and an output terminal (node 28, Fig. 4) coupled to a gate of the second transistor (22, Fig. 4).

Regarding to claim 39, Gonzalez. disclosed, in Figure 4 and respective portion of the specification, the memory device, which is the inverter, further comprises:

a third transistor (26, Fig. 4) of the first conductivity type (n-type) having a gate coupled to the drain (node 20) of the first transistor (10) and a source coupled to receive the first voltage (Vss or ground); and

a fourth transistor (24, Fig. 4) of the second conductivity type (p-type) having a gate coupled to the drain (at node 20) of the first transistor (10, figure 4), a source coupled to receive the second voltage (Vcc) and a drain (node 28) coupled to the drain the third transistor (26, figure 4).

Regarding claim 46, Gonzalez. discloses, in Figure 4 and respective portion of the specification, a 4T-SRAM cell in a SRAM array having pairs of a first and second bit line, and a first and second word line, comprising (see figure 4):

a first transistor (10, Fig. 4) of a first conductivity type (n-type) having a gate (the gate that connects to 16) coupled to a word line (WL) and a source (12) coupled to a bit line;

a second transistor (26, Fig. 4) of the first conductivity type (n-type) having a gate (the gate that connects to node 20) coupled to a drain (connected to 28) of the first transistor (10, figure 4) and a source (the source of 26) coupled to receive a first voltage (ground);

a third transistor (22, Fig. 4) of a second conductivity type (p-type) having a gate coupled to a drain (the connection at node 28) of the second transistor (26, figure 4), a source coupled to receive a second voltage (Vcc) and a drain (the connection at node 20) coupled to the drain of the first transistor (10, figure 4); and

a fourth transistor (24, Fig. 4) of the second conductivity type (p-type) having a gate (see node 20) coupled to one of the second word lines, a source (the connection at Vcc) coupled to one of the second bit lines and a drain (the connection at node 28) coupled to the gate of the third transistor (22, figure 4).

Regarding to claim 47, Gonzalez. disclosed, in Fig. 4 and respective portion of the specification, the 4T-SRAM cell which is the bulks of the first transistor (10, Fig. 4) and fourth transistor (24, Fig. 4) are respectively coupled to receive the first voltage (Vss or ground) and second voltage (Vcc).

Regarding to claim 48, Gonzalez. disclosed, in Fig. 4 and respective portion of the specification, the 4T-SRAM cell which is the first conductivity type (transistors 10, 26 in figures 4 are n-type) and second conductivity types (transistors 22, 24 in figures 4 are p-type) are respectively N and P type.

Allowable Subject Matter

6. Claims 2-13, 17-23, 25-36 and 40-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 2, the prior art of record do not disclose or suggest the first transistor further comprises a bulk coupled to receive a third voltage.

Regarding claim 5, the prior art of record do not disclose or suggest the second transistor further comprises a bulk coupled to receive a third voltage.

Regarding claim 8, the prior art of record do not disclose or suggest the first transistor further comprises a bulk coupled to receive the first voltage.

Regarding claim 11, the prior art of record do not disclose or suggest the second transistor further comprises a bulk coupled to receive the first voltage.

Regarding claim 17, the prior art of record do not disclose or suggest the first and third transistor each comprise a bulk coupled to receive a third voltage.

Regarding claim 20, the prior art of record do not disclose or suggest the first transistor and third transistor comprises a bulk coupled to receive the first voltage.

Regarding claim 23, the prior art of record do not disclose or suggest the diode is formed by a junction between the bulk and drain of the first transistor.

Regarding claim 25, the prior art of record do not disclose or suggest the first transistor further comprises a bulk coupled to receive a third voltage.

Regarding claim 28, the prior art of record do not disclose or suggest the second transistor further comprises a bulk coupled to receive the third voltage.

Regarding claim 31, the prior art of record do not disclose or suggest the first transistor further comprises a bulk coupled to receive the first voltage.

Regarding claim 34, the prior art of record do not disclose or suggest the second transistor further comprises a bulk coupled to receive the first voltage.

Regarding claim 40, the prior art of record do not disclose or suggest the first and third transistors each comprise a bulk coupled to receive a third voltage.

Regarding claim 43, the prior art of record do not disclose or suggest the first and third transistors each comprise a bulk coupled to receive the first voltage.

Regarding claim 45, the prior art of record do not disclose or suggest the diode is formed by a junction between the bulk and drain the first transistor.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sywyk et al. (US. 6,005,796) disclosed the memory cell is dedicated for writing operation and the other port of the memory cell is dedicated for reading operation.

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PML
May 28 2004

Pho M. Luu
Patent Examiner
Art Unit 2824